Q.P. Code: 16EC402 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year I Semester Supplementary Examinations August-2021

SWITCHING THEORY AND LOGIC DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Perform the following i) Subtraction by using 10's complement for the given 3456 - 245. ii)Subtraction by using 2's complement for the given 111001-1010.	6M
	b	i) State Duality theorem. List Boolean laws and their Duals. ii) Simplify the following Boolean expressions to minimum no. of literals. (BC'+A'D)(AB'+CD')	6M

OR

2	a	i) Perform the following using BCD arithmetic $(79)_{10} + (177)_{10}$ ii)Convert the following to gray code $(BC54)_{16}$	6M
	b	Write expressing in canonical form F = (A+B) (B+C)	6M

UNIT-II

3	a	Minimize the following Boolean function using K-Map $F(A,B,C,D)=\sum(1,3,7,11,15)+d(0,2,5)$	6M
	b	Simplify the following Boolean function for minimal POS form using K-map F(X,Y,Z) = X'YZ + XY'Z' + XYZ + XYZ	6M

OR

4	a	Minimize the given Boolean function $F(A,B,C,D) = \Sigma\ m(0,1,2,3,6,7,13,15)$ using tabulation method and implement using basic gates.	7M
	b	Implement the following Boolean equation using only NAND gates Y=AB+CDE+F.	5M

UNIT-III

5	a	Design & implement a 4-bit Binary-To-Gray code converter.	6M
	b	Design & implement Full Adder using Decoder.	6M

OR

6	a	What is encoder? Design octal to binary encoder.	5M
	b	Explain Carry Look Ahead Adder circuit with the help of logic diagram.	7M

UNIT-IV

7	a	Design D Flip Flop by using SR Flip Flop and draw the timing diagram.	6M
	b	With a neat sketch explain MOD 6 Johnson counter using D FF.	6M

OR

8	a	Draw the circuit of JK flip flop using NAND gates and explain its operation.	6M
	b	Design a binary counter having repeated binary sequence using JK flip flops: 0,1,2,4,5,6.	6M

UNIT-V

9	a	Implement the following Boolean function using PLA $F_1(w,x,y,z) = \Sigma m(0,1,3,5,9,13)$ $F_2(w,x,y,z)) = \Sigma m(0,2,4,5,7,9,11,15$	6M
	b	Discuss Mealy & Moore Machine models of sequential machines.	6M

OR

10	a	Give the logic implementation of a 32x4 bit ROM using a decoder of a suitable figure.	6M
	b	Differentiate among ROM, PROM, DROM, EPROM, EEPROM, and RAM.	6M

*** END ***